

4 CHANNEL LOW CAPACITANCE TVS DIODE ARRAY

Product Summary

V _{BR (MIN)}	I _{PP (MAX)}	C _{T (TYP)}
5.5V	3	0.45pF

Description

The D3V3X4U10LP is a high-performance device suitable for protecting four high speed I/Os. These devices are assembled in U-DFN2510-10 packages and have high ESD surge capability, low ESD clamping voltage and Ultra-low capacitance.

Applications

Typically used at high-speed ports such as USB 3.0, USB 3.1, Serial ATA, Display port.

Features

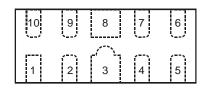
- Clamping Voltage: 6V at 16A IEC6100-4-2
- IEC61000-4-2 (ESD): Air ±8kV, Contact ±8kV
- IEC61000-4-5 (Lightning): 3A (8/20µs)
- 4 Channels of ESD Protection
- Ultra-low Channel Input Capacitance of 0.45pF Typical
- TLP Dynamic Resistance: 0.3Ω
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)

Mechanical Data

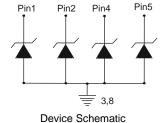
- Case: U-DFN2510-10
- Case Material: Molded Plastic, "Green" Molding Compound.
 UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: NiPdAu over Copper Leadframe (Lead Free Plating).
 Solderable per MIL-STD-202, Method 208 (4)
- Weight: 0.038 grams (Approximate)

U-DFN2510-10

Pin#	Description
1, 2, 4, 5	I/O
6, 7, 9, 10	No Connection
3, 8	Vss



Pin Description (Top View)



Ordering Information (Note 4)

Product	Compliance	Marking	Reel Size (inches)	Tape Width (mm)	Quantity per Reel
D3V3X4U10LP-7	Standard	MU2	7	8	3,000/Tape & Reel

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information

U-DFN2510-10

MU2 YM

MU2 = Product Type Marking Code YM = Date Code Marking Y = Year (ex: E = 2017) M = Month (ex: 9 = September)

Date Code Kev

_	Date Code ite						
	Year	2016	2017	2018	2019	2020	2021
	Code	D	E	F	G	Н	I

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	0	N	D



Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	Condition
Peak Pulse Current, per IEC61000-4-5	I _{PP}	3	Α	I/O to V _{SS} , 8/20µs
Peak Pulse Power, per IEC61000-4-5	P _{PP}	18	W	I/O to V _{SS} , 8/20µs
ESD Protection – Contact Discharge, per IEC61000-4-2	V _{ESD_CONTACT}	±8	kV	I/O to V _{SS}
ESD Protection – Air Discharge, per IEC61000-4-2	V _{ESD_AIR}	±8	kV	I/O to V _{SS}

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation Typical (Note 5)	P _D	350	mW
Thermal Resistance, Junction to Ambient Typical (Note 5)	$R_{ hetaJA}$	360	°C/W
Operating and Storage Temperature Range	T_J , T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition
Reverse Working Voltage	V_{RWM}	_	_	3.3	V	_
Reverse Current	I _R	_	_	1.0	μA	$V_R = 3.3V$, I/O to V_{SS}
Reverse Breakdown Voltage	V_{BR}	5.5	6.2	_	V	I _R = 1mA, I/O to V _{SS}
Forward Clamping Voltage	V _F	-1.0	-0.85	_	V	$I_F = -15$ mA, I/O to V_{SS}
Holding Reverse Voltage	V _{HOLD}	_	1.3	_	V	I/O to V _{SS}
Reverse Clamping Voltage (Note 6)	Vc	_	3	_	V	$I_{PP} = 3A$, I/O to V_{SS} , 8/20 μ s
Clamping Voltage (Note 7)	Vc	_	6	_	V	TLP, 16A, t _P = 100ns, I/O to V _{SS}
Clamping Voltage (Note 7)	Vc	_	5	_	V	TLP, -16A, $t_P = 100$ ns, I/O to V_{SS}
Dynamic Reverse Resistance	R _{DIF-R}	_	0.3	_	Ω	TLP, 10A, $t_P = 100$ ns, I/O to V_{SS}
Dynamic Forward Resistance	R _{DIF-F}	_	0.2	_	Ω	TLP, 10A, t _P = 100ns, V _{SS} to I/O
Channel Input Capacitance	C _{I/O}	_	0.45	_	pF	$V_{I/O} = 0V, V_{SS} = 0V, f = 1MHz$

Notes:

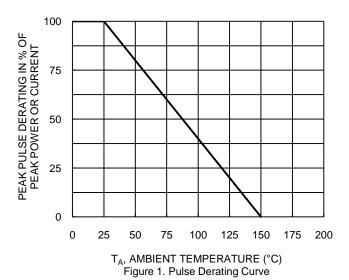
^{5.} Device mounted on FR-4 PCB pad layout (2oz copper) as shown on Diodes Incorporated's suggested pad layout, which can be found on our website at http://www.diodes.com/package-outlines.html.

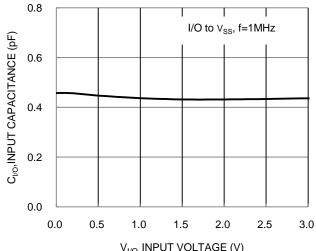
^{6.} Clamping voltage value is based on an $8x20\mu s$ peak pulse current (IPP) waveform.

^{7.} Clamping voltage value is based on a TLP model. TLP conditions: Z_0 =50 Ω , t_P = 100ns, t_P = 1ns, averageing window; t1=70ns to t2=90ns.

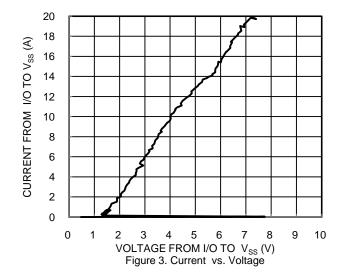








 $\label{eq:V_I/O_INPUT VOLTAGE} V_{I/O_I} \text{INPUT VOLTAGE (V)} \\ \text{Figure 2. Input Capacitance vs. Input Voltage}$

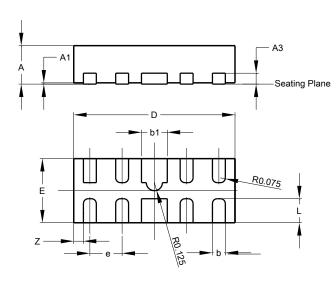




Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN2510-10

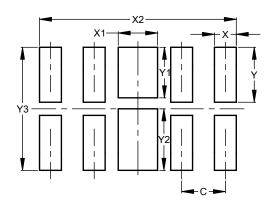


U-DFN2510-10							
Dim	Min	Max	Тур				
Α	0.545	0.605	0.575				
A 1	0.00	0.05	0.03				
A3	-	-	0.13				
b	0.15	0.25	0.20				
b1	035	0.45	0.40				
D	2.450	2.575	2.500				
е	-	-	0.50				
Е	0.950	1.075	1.000				
L	0.325	0.425	0.375				
Z	-	-	0.150				
All Dimensions in mm							

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN2510-10



Dimensions	Value (in mm)
С	0.500
Х	0.250
X1	0.450
X2	2.250
Y	0.625
Y1	0.575
Y2	0.700
Y3	1.400



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