

ADP1043A Daughter Card Evaluation Board

ADP1043ADC1-EVALZ

PRD1274

FEATURES

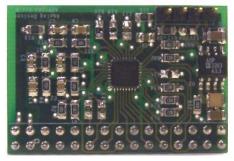
ADP1043A Daughter Card with I2C interface Retrofit controller to any topology or existing design Software GUI Low component count

ADP1043A EVALUATION BOARD OVERVIEW

The daughter card evaluation board allows the ADP1043A to be quickly evaluated in any existing switching power supply application. Using the daughter card and its accompanying software, the IC can be interfaced to any PC running Windows 2000/NT/XP/Vista via the computers USB port.

The daughter card can be connected to any existing ADP1043A evaluation board or reference design.

It can also be connected to any power supply as a replacement for the existing controller. The daughter card has a connector through which the pin outs of the ADP1043A can be probed. The software GUI allows control and read/write functionality of the ADP1043 internal registers to modify, for example, the PWM settings or over current protection limits.



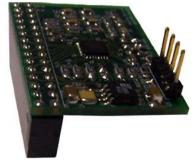


Figure 1 - Daughter card with pin outs of ADP1043A



Rev. 1.0

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TABLE OF CONTENTS

| Features | 1 |
|--|-----|
| EVALUATION BOARD HARDWARE | 3 |
| CONNECTORS | 4 |
| REFURNISHING AND EXISTING DESIGN WITH ADP1043A DAUGHTER CARD | 5 |
| Additional key points and checklist: | 7 |
| SCHEMATIC | 8 |
| LAYOUT | 9 |
| BILL OF MATERIALS | .12 |
| Notes | .13 |

REVISION HISTORY

09/15/2010 - Revision 1.0: SPM 09/21/2010 - Revision 2.0: SPM with MS feedback 10/04/2010 - Revision 3.0: MS feedback implemented

| Card | SHAREi | SCL | FLAGIN | PGOOD1 | OUTAUX | OUTC | OUTA | ACSNS | SR2 | CS2+ | VS1 | GATE | VS3- | +3.3V | +12V |
|-------------------------------------|------------|---------|---------|------------|----------|-----------|-----------|----------|----------|-----------|-----------|----------|-----------|----------|-----------|
| 3A Daughter Connector | 0 2 | 04 | 90 | 80 | O 10 | O 12 | 0 14 | O 16 | O 18 | O 20 | 0 22 | O 24 | O 26 | O 28 | 0 30 |
| ADP1043A Daughter Card Connector | SHAREO 1 O | SDA 3 O | RTD 5 O | PG00D2 7 O | D 6 NO S | OUTD 11 O | OUTB 13 O | CS1 15 O | SR1 17 O | CS2- 19 O | PGND 21 O | VS2 23 O | V53+ 25 O | +5V 27 O | AGND 29 O |
| 4 3 2 1 | | | | | | | | | | | | | | | |

Figure 2 - Simplified Block Diagram

EVALUATION BOARD HARDWARE

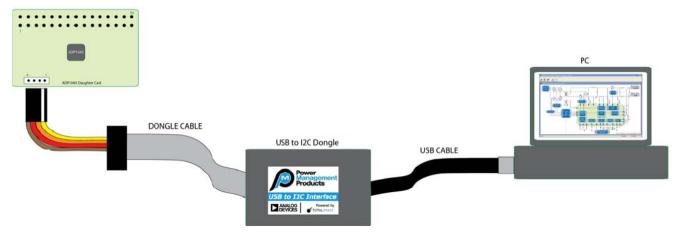


Figure 3 - Connection diagram of daughter card to PC via I2C interface (USB dongle)

CONNECTORS

The pin outs of the USB dongle are given below:



| Pin | Evaluation Board Function | | | | |
|-----|----------------------------------|--|--|--|--|
| 1 | 5V | | | | |
| 2 | SCL | | | | |
| 3 | SDA | | | | |
| 4 | Ground | | | | |

Table 1 - I2C connector pin out descriptions

Figure 4 – I2C connector (pin1 on left)

| ADP1043A Daughter Card Connector | | | | | | | | |
|-------------------------------------|----|---|------|--------|--|--|--|--|
| SHAREo | 1 | 0 | 0 2 | SHAREi | | | | |
| SDA | 3 | 0 | 04 | SCL | | | | |
| RTD | 5 | 0 | 06 | FLAGIN | | | | |
| PGOOD2 | 7 | 0 | 08 | PGOOD1 | | | | |
| PS_ON | 9 | 0 | O 10 | OUTAUX | | | | |
| OUTD | 11 | 0 | O 12 | OUTC | | | | |
| OUTB | 13 | 0 | O 14 | OUTA | | | | |
| CS1 | 15 | 0 | O 16 | ACSNS | | | | |
| SR1 | 17 | 0 | O 18 | SR2 | | | | |
| CS2- | 19 | 0 | O 20 | CS2+ | | | | |
| PGND | 21 | 0 | O 22 | VS1 | | | | |
| VS2 | 23 | 0 | O 24 | GATE | | | | |
| VS3+ | 25 | 0 | O 26 | VS3- | | | | |
| +5V | 27 | 0 | O 28 | +3.3V | | | | |
| AGND | 29 | 0 | O 30 | +12V | | | | |

Figure 5 - Detailed description of pin outs

REFURNISHING AND EXISTING DESIGN WITH ADP1043A DAUGHTER CARD

To evaluate the IC with an existing power supply, a jumper cable can be used. Figure 6 and Figure 7 demonstrate how a jumper cable is connected on one end to the daughter card and the other end to the respective function of the pin on the power supply.

Care must be taken to ensure that the traces/wires that are connected at their respective sensing points are short and are not routed through any high frequency traces (switching nodes) of the power stage that would result in poor signal integrity due to noise injection or EMI. A spread of wires must definitely be avoided as this increases the probability of injected noise due to bigger loop areas and common impedance coupling between the power ground and the analog and digital grounds.

Note: The ADP1043A provides control and logic signals for the power switches. External drivers need to be used to turn on/off the switches in the power stage of the design.

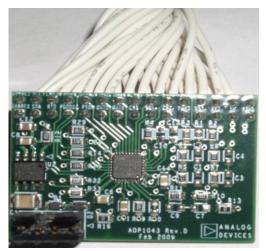


Figure 6 – Daughter card connection

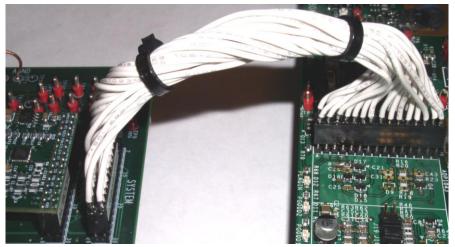


Figure 7 – Example of a retrofitted system with daughter card on left and power stage on the right.

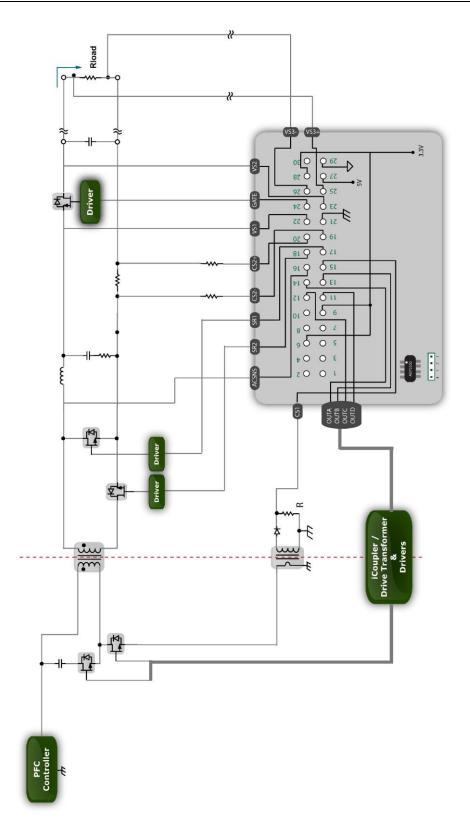


Figure 8 - Block diagram of power stage and interconnection with daughter card

ADDITIONAL KEY POINTS AND CHECKLIST:

- The daughter card is powered using the USB cable. The 3.3V LDO present on the PCB converts the 5V to 3.3V which supplies power to the ADP1043A. Alternately an isolated power supply 5V or 12V (referenced to AGND) may be used and connected to pins on the daughter card. The I2C connecter also has the SDA and SCL pins which are used for serial communication to the ADP1043A using the software GUI.
- 2. The RTD pin is referenced to AGND and the thermistor must be ideally placed close to the hottest part of the power stage for monitoring over temperature. Leave open if not used.
- 3. Connect the FLAGIN pin to 3.3V if this function is not required or set the flag to ignore in the Flags and Settings window in the GUI.
- 4. Connect PS_ON to 3.3V using a switch or permanently connected to 3.3V. If permanently connected then the power supply can be turned on using software PS_ON in the GUI.
- 5. OUTA, OUTB, OUTC, OUTD, and OUTAUX, are the PWMs used for the primary power switches while SR1 and SR2 are the PWMs used for the secondary side synchronous rectifiers.
- 6. The ACSNS flag is set when the ACSNS pin reads a value less than 0.45V. The flag is configurable.
- 7. CS2+ and CS2- (differential input) must be connected across the current sense resistor. Care must be taken not to exceed 150mV as it exceeds the maximum range of the ADC.
- 8. The voltage dividers for sensing the output voltage (VS1, VS2, and VS3) are on the daughter card. VS1 and VS2 are referenced to PGND whereas VS3+ and VS3- are differential inputs. VS3- must be connected to PGND. The voltage divider must be configured to provide 1V at the divider at the nominal output voltage to provide enough range for trimming. Care must be taken not to exceed 1.55V as it exceeds the maximum range of the ADC.
- 9. The GATE pin must be left open if the OrFET functionality is not used.
- 10. The CS1 signal is referenced to PGND. Care must be taken not to exceed 1.55V as it exceeds the maximum range of the ADC. The CS1 fast OCP comparator is set to trip at 1.2V. When using a current sense transformer the resistor R (see *Figure 8*) is sized by the equation: $R = V_CS1 \times N2/(N1 \times I_{PRIMARY_PEAK})$.
- 11. An external 12V connection can be provided to pin 30 of the daughter card to provide power for the switch drivers.

SCHEMATIC

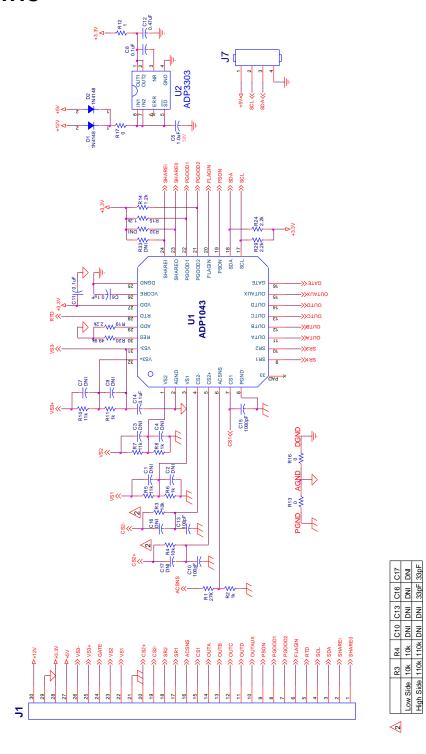


Figure 9 – Daughter card schematic

1: R3, R4, R5, R6, R7, R8, R10, R11 ARE 0.1% 25ppm UNLESS OTHERWISE SPECIFIED.

NOTES:

LAYOUT

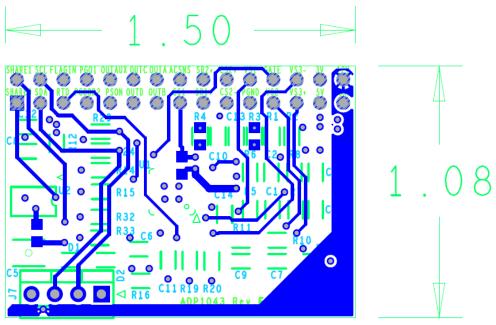


Figure 10 - Bottom Layer, dimensions in inches

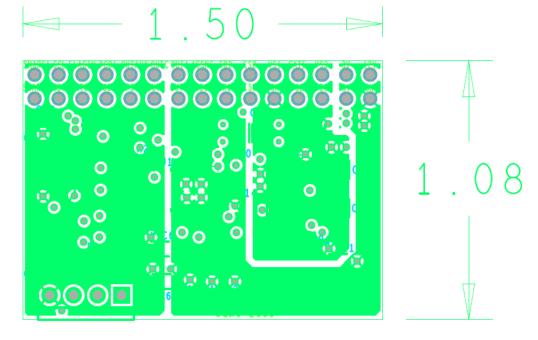


Figure 11 - GND Layer, dimensions in inches

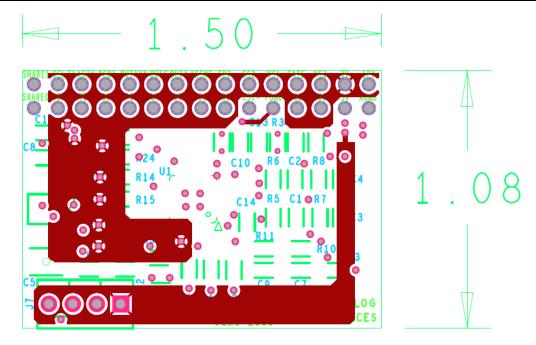


Figure 12 - Power Layer, dimensions in inches

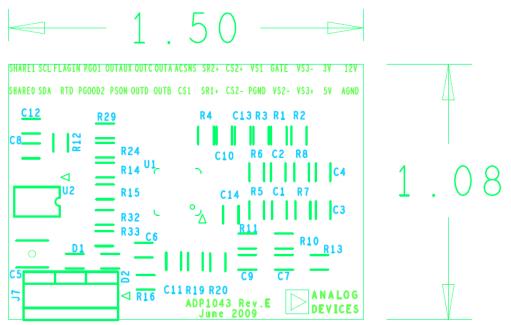


Figure 13 - Figure 53 - Silkscreen Layer, dimensions in inches

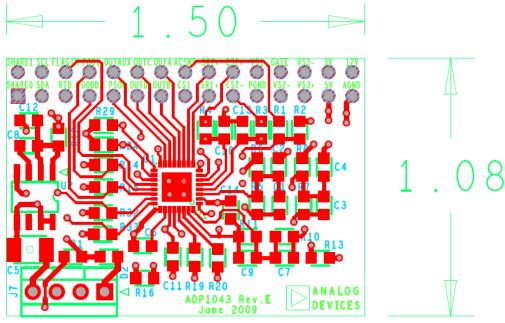


Figure 14 - Figure 54 - Figure 53 - Top Layer, dimensions in inches

BILL OF MATERIALS

| Item | Part Ref | Part Description | Package | Manufacturer | Mfg Part No |
|------|----------|---|-------------|-----------------------------|--------------------|
| 1 | C1 | DNI | | Murata | GRM32RR71H105KA01L |
| 2 | C2 | DNI | | | |
| 3 | C3 | DNI | | | |
| 4 | C4 | DNI | | | |
| 5 | C5 | CAPACITOR CERAMIC 1.0UF 50V 10% X7R | 1210 |) Murata | GRM32RR71H105KA01L |
| 6 | C6 | CAPACITOR CERAMIC 0.1UF 10% 50V X7R | 805 | AVX | 08055C104KAT2A |
| 7 | C7 | DNI | | | |
| 8 | C8 | CAPACITOR CERAMIC 0.1UF 10% 50V X7R | 805 | AVX | 08055C104KAT2A |
| 9 | C9 | DNI | | | |
| 10 | C10 | DNI | | | |
| 11 | C11 | CAPACITOR CERAMIC 0.1UF 10% 50V X7R | 805 | AVX | 08055C104KAT2A |
| 12 | C12 | CAPACITOR CERAMIC 0.47UF 5% 17V X7R | 805 | AVX | 0805YC474JAT2A |
| 13 | C13 | DNI | | | |
| 14 | C14 | CAPACITOR CERAMIC 0.01UF 10% 100V X7R | 805 | AVX | 08051C103KAT2A |
| 15 | C15 | CAPACITOR CERAMIC 1000pF 10% 100V X7R | 603 | Murata | GRM188R72A102KA01D |
| 16 | J1 | CONNETOR HEADER FEMALE 30PS .1" DL TIN | Fmal Socket | Sullins Connector Solutions | PPTC152LFBN-RC |
| 17 | J7 | CONNECTOR HEADER 4POS SGL PCB 30 GOLD | Header-4POS | FCI | 69167-104HLF |
| 18 | R1 | RESISTOR 27.0K OHM 1/8W 1% SMD | 805 | Any | |
| 19 | R2 | RESISTOR 1.00K OHM 1/8W 1% SMD | 805 | Any | |
| 20 | R3 | RESISTOR 10.0K OHM 1/10W .1% +/-25ppm SMD | 805 | Any | |
| 21 | R4 | RESISTOR 10.0K OHM 1/10W .1% +/-25ppm SMD | 805 | 5 Any | |
| 22 | R5 | RESISTOR 11.0K OHM 1/10W .1% +/-25ppm SMD | 805 | Any | |
| 23 | R6 | RESISTOR 1.00K OHM 1/10W .1% +/-25ppm SMD | 805 | Any | |
| 24 | R7 | RESISTOR 11.0K OHM 1/10W .1% +/-25ppm SMD | 805 | Any | |
| 25 | R8 | RESISTOR 1.00K OHM 1/10W .1% +/-25ppm SMD | 805 | 5 Any | |
| 26 | R10 | RESISTOR 11.0K OHM 1/10W .1% +/-25ppm SMD | 805 | 5 Any | |
| 27 | R11 | RESISTOR 1.00K OHM 1/10W .1% +/-25ppm SMD | 805 | 5 Any | |
| 28 | R12 | RESISTOR 0.0 OHM 1/8W 5% SMD | 805 | 5 Any | |
| 29 | R13 | RESISTOR 0.0 OHM 1/8W 5% SMD | 805 | 5 Any | |
| 30 | R14 | RESISTOR 1.00K OHM 1/8W 1% SMD | 805 | 5 Any | |
| 31 | R15 | RESISTOR 1.00K OHM 1/8W 1% SMD | 805 | Any | |
| 32 | R16 | RESISTOR 0.0 OHM 1/8W 5% SMD | | 5 Any | |
| 33 | R17 | RESISTOR 0.0 OHM 1/8W 5% SMD | 805 | Any | |
| 34 | R18 | DNI | | | |
| 35 | R19 | RESISTOR 10.0K OHM 1/8W 1% SMD | 805 | 5 Any | |
| 36 | R20 | RESISTOR 49.9K OHM 1/8W 1% SMD | 805 | 5 Any | |
| 37 | R24 | RESISTOR 2.20K OHM 1/8W 1% SMD | 805 | 5 Any | |
| 38 | R29 | RESISTOR 2.20K OHM 1/8W 1% SMD | 805 | Any | |
| 39 | R32 | DNI | | | |
| 40 | R33 | DNI | | | |
| 41 | U1 | I.C. Secondary Side Power Supply Controller | LFCSP-32 | ADP1043A | Analog Devices |
| 42 | U2 | I.C. LDO LINEAR REGULATOR 200MA 3.3V | SOIC-8 | ADP3303 | Analog Devices |

Table 2 - Bill of Materials

NOTES



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